ISO 9001 Registered

IMP5121

27-Line SCSI Terminator

–Plug and Play

DESCRIPTION

The IMP5121 Plug and Play terminator represents next-generation technology for SCSI termination applications. The low-voltage BiCMOS architecture employed in its design offers performance superior to older passive and active techniques. IMP's architecture employs high-speed adaptive elements for each channel, providing the fastest response possible. The channel bandwidth is typically 35MHz. The IMP5121 compares favorably to older linear regulator approaches whose bandwidth's are dominated by the output compensation capacitor and are limited to the 500KHz bandwidth region (see further discussion in the Functional Description section). IMP's architecture also eliminates the output compensation capacitor required in earlier terminator designs. Each is approved for use with SCSI-1, -2, -3, ULTRA and beyond — providing the highest performance alternative available today.

Another key improvement of the IMP5121 products lies in their ability to insure reliable, error free communications even in systems which do not necessarily adhere to recommended SCSI hardware design guidelines, such as the use of improper cable lengths and impedances. Frequently, this situation is not controlled by the peripheral or host designer and, when problems occur, they are the first to be made aware of these problems. The IMP5121 architecture is much more tolerant of marginal system integrations.

Recognizing the needs of portable and configurable peripherals, the IMP5121 has a TTL compatible sleep/disable mode. Quiescent current is typically less than 375µA in this mode, while the output capacitance is less than 3pF.

Reduced component count is also inherent in the IMP5121 architecture. Traditional termination techniques require large stabilization and transient protection capacitors of up to 20µF in value and size. The IMP5121 architecture does not require these components, allowing all the cost savings associated with inventory, board space, assembly, reliability, and component costs.

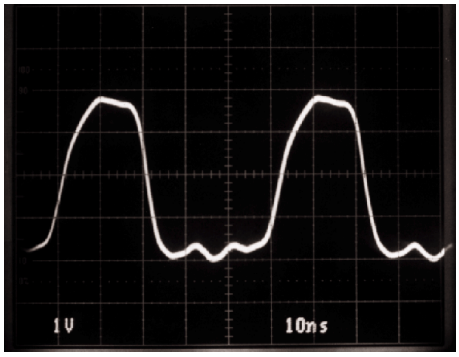
The IMP5121 has multiple disables for full Plug and Play SCSI capability for Host Bus Adapters with 3 SCSI connectors. It also splits the upper 9 termination lines for mixing 16-bit (wide) and 8-bit (narrow) buses with minimal board trace capacitance.

KEY FEATURES

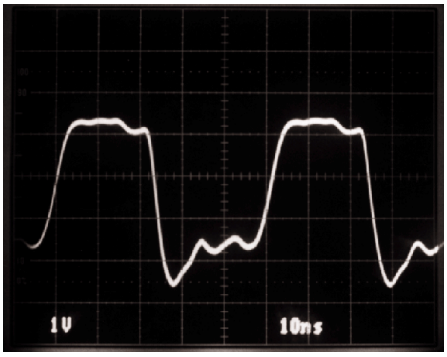
- ULTRA-FAST RESPONSE FOR FAST-20 SCSI APPLICATIONS
- PLUG AND PLAY SCSI FOR HOST BUS ADAPTERS WITH 3 SCSI CONNECTORS
- SPLIT DISCONNECT FOR MIXING 16-BIT (WIDE) OR 8-BIT (NARROW) BUSES
- 35MHz CHANNEL BANDWIDTH
- 3.3V OPERATION
- LESS THAN 3pF (TYP.) OUTPUT CAPACITANCE
- SLEEP-MODE CURRENT LESS THAN 375µA
- HOT-SWAP COMPATIBLE
- NO EXTERNAL COMPENSATION CAPACITORS
- COMPATIBLE WITH ACTIVE NEGATION DRIVERS (60mA / CHANNEL)
- SUPERIOR REPLACEMENT FOR THE UCC5621

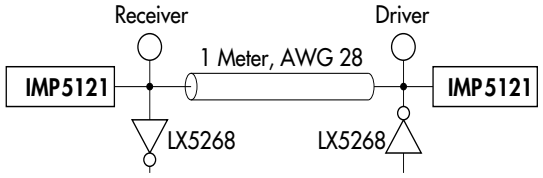
PRODUCT HIGHLIGHT

RECEIVING WAVEFORM - 20MHz



DRIVING WAVEFORM - 20MHz





PACKAGE ORDER INFO

T_J (°C)	PW Plastic TSSOP 56-pin	DB Plastic SSOP 44-pin
0 to 125	IMP5121CPW	IMP5121CDB

Note: Available in Tape & Reel.
Append the letter "T" to part number. (i.e. IMP5121CDBT)

ABSOLUTE MAXIMUM RATINGS (Note 1)

TermPwr Voltage 7V
Continuous Output Voltage Range ..... 0 to 5.5V
Continuous Disable Voltage Range ..... 0 to 5.5V
Operating Junction Temperature
Plastic (PW & DB Packages) ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Solder Temperature (Soldering, 10 seconds) ..... 300°C

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DATA

PW PACKAGE:

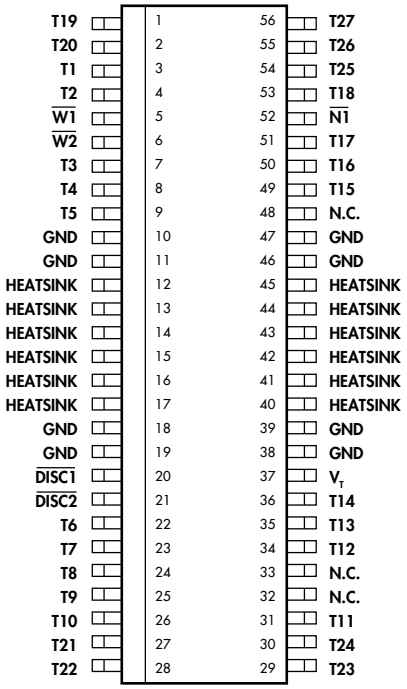
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Θ_{JA} ..... 50°C/W

DB PACKAGE:

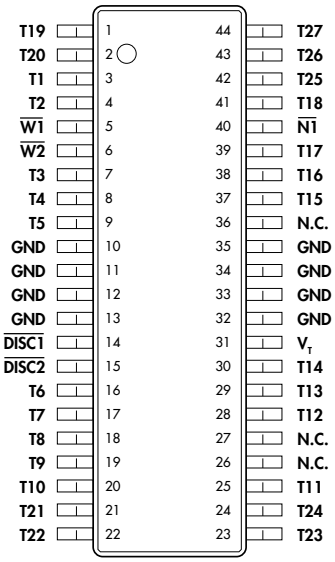
THERMAL RESISTANCE-JUNCTION TO AMBIENT, Θ_{JA} ..... 50°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

PACKAGE PIN OUTS



PW PACKAGE
(Top View)



DB PACKAGE
(Top View)

RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Termination Voltage	V_{TERM}	3.0		5.5	V
High Level Disable Input Voltage	V_{IH}	2		V_{TERM}	V
Low Level Disable Input Voltage	V_{IL}	0		0.8	V
Operating Virtual Junction Temperature Range					
IMP5121C		0		125	°C

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

Term Power = 4.75V unless otherwise specified. Unless otherwise specified, these specifications apply at the recommended operating ambient temperature of T_A = 25°C. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.

Parameter		Symbol	Test Conditions	IMP5121			Units
				Min.	Typ.	Max.	
Output High Voltage		V_{OUT}		2.65	2.85		V
TermPwr Supply Current		I_{CC}	All data lines = open		12	18	mA
			All data lines = 0.5V		635	670	mA
			Disable Pins 1, 2, $\overline{W1}$, $\overline{W2}$ & $\overline{N1}$ < 0.8V		375		µA
Output Current		I_{OUT}	V_{OUT} = 0.5V	-21	-23	-24	mA
Disable Input Current	$\overline{DISC1}$	I_{IN}	$\overline{DISC1}$ = 0V		-20		µA
			$\overline{DISC1}$ = 4.75V		10		nA
	$\overline{DISC2}$		$\overline{DISC2}$ = 0V		-20		µA
			$\overline{DISC2}$ = 4.75V		10		nA
Output Leakage Current			$\overline{DISC1}$ and $\overline{DISC2}$= < 0.8V, V_O = 0.5V		10		nA
Capacitance in Disabled Mode		C_{OUT}	V_{OUT} = 0V, frequency = 1MHz		3		pF
Channel Bandwidth		BW			35		MHz
Termination Sink Current, per Channel		I_{SINK}	V_{OUT} = 4V		60		mA

FUNCTIONAL DESCRIPTION

Cable transmission theory suggests that in order to optimize signal speed and quality, the termination should act both as an ideal voltage reference when the line is released (de-asserted) and as an ideal current source when the line is active (asserted). Common active terminators, which consist of Linear Regulators in series with resistors (typically 110Ω), are a compromise. As the line voltage increases, the amount of current decreases linearly by the equation V = I * R. The IMP5121, with its unique new architecture, applies the maximum amount of current regardless of line voltage until the termination high threshold (2.85V) is reached.

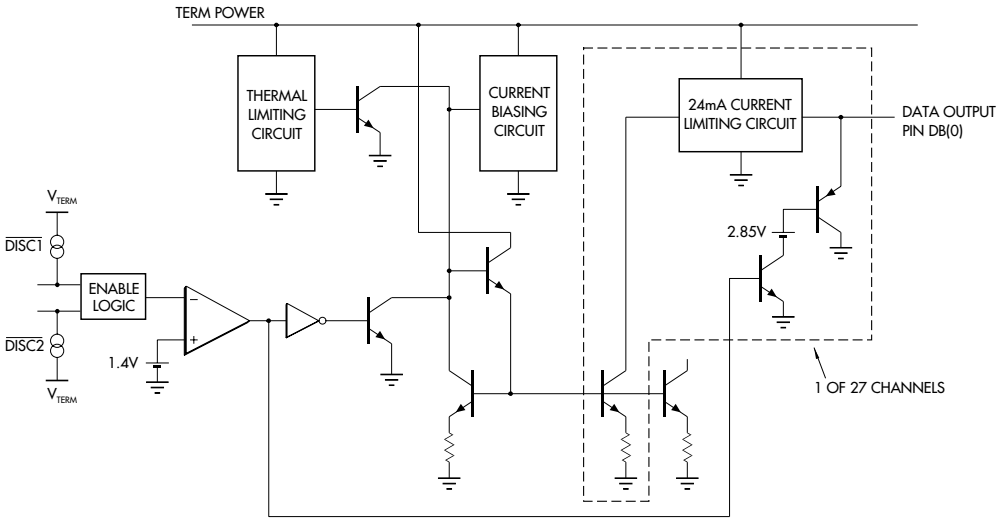
Power Up / Power Down Function Table

$\overline{DISC1}$	$\overline{DISC2}$	$\overline{W1}$	$\overline{W2}$	$\overline{N1}$	T1-T18	T19-T27
H	L	DC	DC	DC	Enabled	Disabled
L	H	DC	DC	DC	Disabled	Enabled
L	L	DC	DC	DC	Disabled	Disabled
H	H	H	H	H	Enabled	Enabled
H	H	H	H	L	Enabled	Enabled
H	H	H	L	H	Enabled	Enabled
H	H	H	L	L	Disabled	Enabled
H	H	L	H	H	Enabled	Enabled
H	H	L	H	L	Disabled	Enabled
H	H	L	L	H	Disabled	Disabled
H	H	L	L	L	Disabled	Disabled

Acting as a near ideal line terminator, the IMP5121 closely reproduces the optimum case when the device is enabled. To enable the device the $\overline{DISC1}$ and $\overline{DISC2}$ pins must be driven per the above table. During this mode of operation, quiescent current is 12mA and the device will respond to line demands by delivering 24mA on assertion and by imposing 2.85V on de-assertion. Disable mode places the device in a sleep state, where a meager 375µA of quiescent current is consumed. Additionally, all outputs are in a Hi-Z (impedance) state. Sleep mode can be used for power conservation or to completely eliminate the terminator from the SCSI chain. In the second case, termination node capacitance is important to consider. The terminator will appear as a parasitic distributed capacitance on the line, which can detract from bus performance. For this reason, the IMP5121 has been optimized to have only 4pF of capacitance per output in the sleep state.

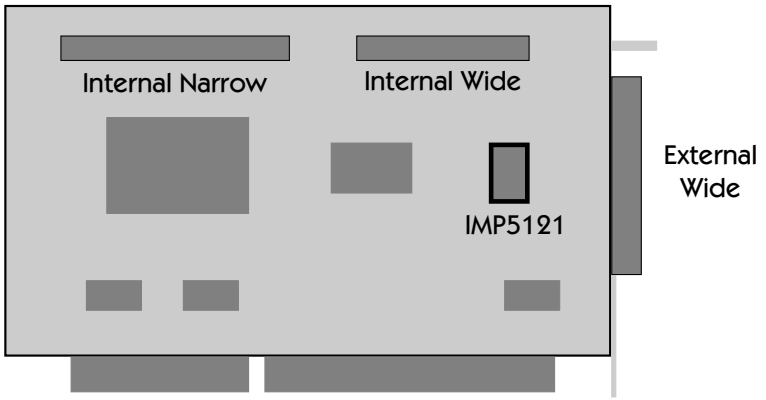
An additional feature of the IMP5121 is its compatibility with active negation drivers. The device handles up to 60mA of sink current for drivers which exceed the 2.85V output high.

BLOCK DIAGRAM



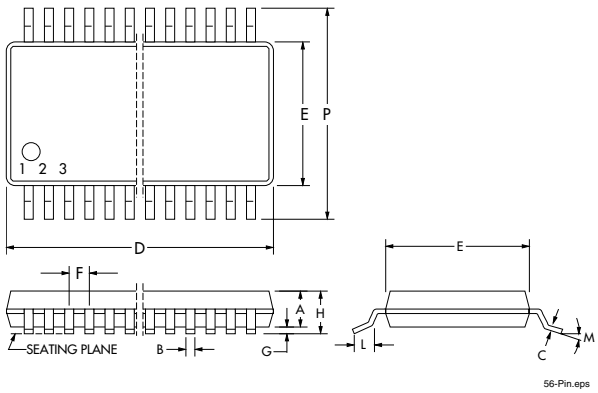
PLUG AND PLAY DIAGRAM

The Plug and Play SCSI auto-termination disabling, connect pin 50 of the External Wide SCSI connector to $\overline{W1}$ of the IMP5121, connect pin 50 of the Internal Wide SCSI connector to $\overline{W2}$ of the IMP5121, and connect pin 22 of the Internal Narrow connector to $\overline{N1}$ of the IMP5121.



PACKAGE DIMENSIONS

PW 56-Pin TSSOP
POWER



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	0.80	1.05	0.032	0.041
B	0.17	0.27	0.007	0.011
C	0.09	0.20	0.004	0.008
D	13.90	14.10	0.547	0.555
E	6.0	6.2	0.236	0.244
F	0.50 BSC		0.02 BSC	
G	0.05	0.15	0.002	0.005
H	—	1.20	—	0.047
L	0.45	0.75	0.018	0.030
M	0°	8°	0°	8°
P	8.1 BSC		0.32 BSC	
***LC**	—	0.10	—	0.004

* Lead Coplanarity

Note 1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.15mm (0.006") on any side. Lead dimension shall not include solder coverage.

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Publication #: 7005
Revision: A
Issue Date: 09/09/99
Type: Product